Selection Guide

Input signals of the interface electronics
Interface electronics from HEIDENHAIN can be connected to encoders with sinusoidal signals of 1 V_{PP} (voltage signals) or 11 μA_{PP} (current signals). Encoders with the serial interfaces EnDat or SSI can also be connected to various interface electronics.

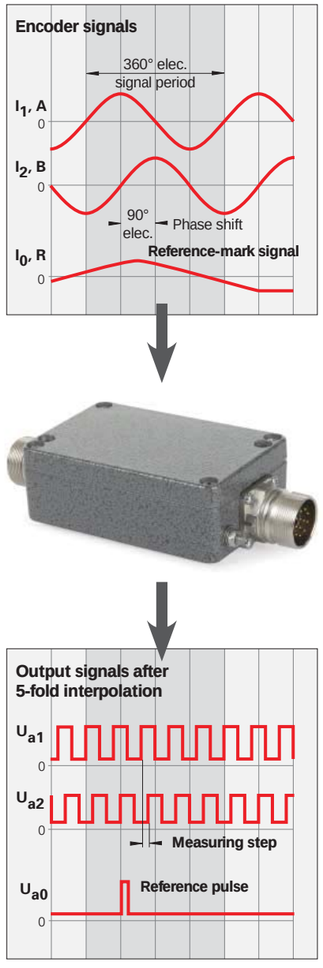
Output signals of the interface electronics
Interface electronics with the following interfaces to the subsequent electronics are available:
- TTL square-wave pulse trains
- EnDat 2.2
- FANUC serial interface
- Mitsubishi High Speed Serial Interface
- PCI bus
- Ethernet
- Profibus

Interpolation of the sinusoidal input signals
In addition to being converted, the sinusoidal encoder signals are also interpolated in the interface electronics. This results in finer measuring steps, leading to an increased positioning accuracy and higher control quality.

Formation of a position value
Some interface electronics have an integrated counting function. Starting from the last reference point set, an absolute position value is formed when the reference mark is traversed, and is output to the subsequent electronics.

Measured value memory
Interface electronics with integrated measured value memory can buffer-save measured values:
IK 220: Total of 8192 measured values
EIB 741: Per input 250000 measured values

Example of 5-fold interpolation



Outputs		Inputs		Design – protection class	Interpolation[1] or subdivision	Model
Interface	Number	Interface	Number			
⊓⊔ TTL	1	∿ 1 V_{PP}	1	Box design – IP 65	5/10-fold	**IBV 101**
					20/25/50/100-fold	**IBV 102**
					Without interpolation	**IBV 600**
					25/50/100/200/400-fold	**IBV 660B**
				Plug design – IP 40	5/10/20/25/50/100-fold	**APE 371**
				Version for integration – IP 00	5/10-fold	**IDP 181**
					20/25/50/100-fold	**IDP 182**
		∿ 11 μA_{PP}	1	Box design – IP 65	5/10-fold	**EXE 101**
					20/25/50/100-fold	**EXE 102**
					Without/5-fold	**EXE 602E**
					25/50/100/200/400-fold	**EXE 660B**
				Version for integration – IP 00	5-fold	**IDP 101**
⊓⊔ TTL/∿ 1 V_{PP} Adjustable	2	∿ 1 V_{PP}	1	Box design – IP 65	2-fold	**IBV 6072**
					5/10-fold	**IBV 6172**
EnDat 2.2	1	∿ 1 V_{PP}	1	Box design – IP 65	≤ 16384-fold subdivision	**EIB 192**
				Plug design – IP 40	≤ 16384-fold subdivision	**EIB 392**
FANUC serial interface	1	∿ 1 V_{PP}	1	Box design – IP 65	≤ 16384-fold subdivision	**EIB 192F**
				Plug design – IP 40	≤ 16384-fold subdivision	**EIB 392F**
Mitsubishi High Speed Serial Interface	1	∿ 1 V_{PP}	1	Box design – IP 65	≤ 16384-fold subdivision	**EIB 192M**
				Plug design – IP 40	≤ 16384-fold subdivision	**EIB 392M**
PCI bus	1	∿ 1 V_{PP} ∿ 11 μA_{PP} EnDat 2.1 / 01 SSI Adjustable	2	Version for integration – IP 00	≤ 4096-fold subdivision	**IK 220**
Ethernet	1	∿ 1 V_{PP} EnDat 2.1 EnDat 2.2 ∿ 11 μA_{PP} upon request Adjustable by software	4	Benchtop design – IP 40	≤ 4096-fold subdivision	**EIB 741**
PROFIBUS DP	1	EnDat	1	Top-hat rail design	–	**PROFIBUS Gateway**

[1] Switchable

Interfaces
Incremental Signals ⊓⊔ TTL

The IBV, EXE, APE and IDP interpolation and digitalizing electronics from HEIDENHAIN convert the sinusoidal output signals from HEIDENHAIN encoders, with or without interpolation, into ⊓⊔ TTL square-wave signals.

The **incremental signals** are transmitted as the square-wave pulse trains U_{a1} and U_{a2}, phase-shifted by 90° elec. The **reference mark signal** consists of one or more reference pulses U_{a0}, which are gated with the incremental signals. In addition, the integrated electronics produce their **inverted signals** $\overline{U_{a1}}$, $\overline{U_{a2}}$ and $\overline{U_{a0}}$ for noise-proof transmission.

The illustrated sequence of output signals—with U_{a2} lagging U_{a1}—applies to the direction of motion shown in the dimension drawing.

The **fault-detection signal** $\overline{U_{aS}}$ indicates fault conditions such as breakage of the power line or failure of the light source. It can be used for such purposes as machine shut-off during automated production.

The distance between two successive edges of the incremental signals U_{a1} and U_{a2} through 1-fold, 2-fold or 4-fold evaluation is one **measuring step.**

The subsequent electronics must be designed to detect each edge of the square-wave pulse. The minimum **edge separation a** listed in the *Specifications* applies to the illustrated input circuitry with a cable length of 1 m, and refers to a measurement at the output of the differential line receiver. Propagation-time differences in cables additionally reduce the edge separation by 0.2 ns per meter of cable length. To prevent counting errors, design the subsequent electronics to process as little as 90 % of the resulting edge separation. The max. permissible **shaft speed** or **traversing velocity** must never be exceeded.

Interface	Square-wave signals ⊓⊔ **TTL**
Incremental signals	**2 TTL square-wave signals U_{a1}, U_{a2}** and their inverted signals **$\overline{U_{a1}}$, $\overline{U_{a2}}$**
Reference-mark signal Pulse width Delay time	**1 or more TTL square-wave pulses U_{a0}** and their inverted pulses **$\overline{U_{a0}}$** 90° elec. (can be switched to 270° elec.) $\lvert t_d \rvert \leq 50$ ns
Fault-detection signal Pulse width	**1 TTL square-wave pulse $\overline{U_{aS}}$** Improper function: LOW (switchable to three-state: U_{a1}/U_{a2} high impedance) Proper function: HIGH $t_S \geq 20$ ms *EXE 602E:* $t_S \geq 250$ µs can be switched to 40 ms
Signal levels	Differential line driver as per EIA standard RS-422 $U_H \geq 2.5$ V at $-I_H = 20$ mA $U_L \leq 0.5$ V at $I_L = 20$ mA
Permissible load	$Z_0 \geq 100\ \Omega$ Between associated outputs $\lvert I_L \rvert \leq 20$ mA Max. load per output $C_{load} \leq 1000$ pF With respect to 0 V Outputs protected against short circuit to 0 V
Switching times (10 % to 90 %)	$t_+ / t_- \leq 30$ ns (typically 10 ns) with 1 m cable and recommended input circuitry
Connecting cable Cable length Propagation time	Shielded HEIDENHAIN cable PUR [4(2 × 0.14 mm²) + (4 × 0.5 mm²)] Max. 100 m ($\overline{U_{aS}}$ max. 50 m) at distributed capacitance 90 pF/m 6 ns/m